Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-8. (Cancelled)

9. (Original) A semiconductor integrated circuit including a plurality of standard cells which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors,

each standard cell of said cell row being provided with at least one first contact region through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential,

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location, and

wherein said expanded regions are formed in spaces which said standard cell can afford.

10. (cancelled)

11. (previously presented) A semiconductor integrated circuit including a plurality of standard cells which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors,

each standard cell of said cell row being provided with at least one first contact region through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential, and

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location.

12. (currently amended) The semiconductor integrated circuit as claimed in claim [[1]] 11 wherein said contact regions of said first substrate continuous region are located in said expanded regions.

13. (currently amended) The semiconductor integrated circuit as claimed in claim [[1]] 11 wherein said expanded regions are formed in spaces which said standard cell can afford.

14. (currently amended) The semiconductor integrated circuit as claimed in claim [[3]] 13 wherein said contact regions of said first substrate continuous region are located in said expanded regions.